**Birla Institute of Technology & Science, Pilani**

**Work Integrated Learning Programmes Division**

**First Semester 2023-2024**

**Comprehensive Examination**

**(EC-3 Regular)**

Course No. : BITS ZG553

Course Title : Real Time Systems

Nature of Exam : Open Book

Pattern of Exam : Typed Only

Weightage : 40%

No. of Pages = 7

# ***No. of Questions = 10***

Duration : 2 ½ Hours

Date of Exam : 24/11/2023(FN)

Note to Students:

1. Please follow all the *Instructions to Candidates* given on the cover page of the answer book.
2. All parts of a question should be answered consecutively. Each answer should start from a fresh page.
3. Assumptions made if any, should be stated clearly at the beginning of your answer.

Validate the below two statements (True/False) with brief justification (use bullet-points):

1. *“Cyclic schedulers do not require storing a precomputed schedule unlike table‐driven schedulers.”*
2. *"The upper bound on achievable utilization improves as the number of tasks in the system being developed increases when RMA is used for scheduling a set of hard real‐time periodic tasks.”* [4]

Q.1 Set (B)  
Validate the below two statements (True/False) with brief justification (use bullet-points):

1. *“Cyclic schedulers do require storing a precomputed schedule unlike table‐driven schedulers.”*
2. *"The upper bound on achievable utilization falls as the number of tasks in the system being developed increases when RMA is used for scheduling a set of hard real‐time periodic tasks.”* [4]

Q.1 Set (C)  
Validate the below two statements (True/False) with brief justification (use bullet-points):

1. *"The upper bound on achievable utilization falls as the number of independent tasks in the system being developed increases when RMA is used for scheduling a set of hard real‐time periodic tasks.*
2. *“Table-driven schedulers do require storing a precomputed schedule like cycle‐driven schedulers.”* [4]



How the scheduling points (time at which the scheduler makes decisions regarding which task is to be run next) for the below two task scheduling algorithms are determined? (i) clock‐driven, (ii) event‐driven. [4]



How the scheduling points (time at which the scheduler makes decisions regarding which task is to be run next) for the below two task scheduling algorithms are determined? (i) Table‐driven, (ii) event‐driven. [4]

Q.2 Set. (C)

How the scheduling points (time at which the scheduler makes decisions regarding which task is to be run next) for the below two task scheduling algorithms are determined? (i) clock‐driven, (ii) table-driven. [4]



Assume that the system has a two-level cache. The L1 cache has a hit rate of 90% and the L2 cache has a hit rate of 95%. The L1 cache access time is 5 ns and access time of main memory is 100 ns. What should be the access time of L2 cache in order to achieve an average memory access time of 6.5 ns? [4]

Assume that the system has a two-level cache. The L2 cache has a hit rate of 95% and the L1 cache has a hit rate of 90%. The L1 cache access time is 5 ns and access time of main memory is 100 ns. What should be the access time of L2 cache in order to achieve an average memory access time of 6.5 ns? [4]



Assume that the system has a two-level cache. The L1 cache has a hit rate of 90% and the L2 cache has a hit rate of 95%. The L1 cache access time is 5 ns and access time of main memory is 100 ns. What should be the access time of L2 cache in order to achieve an average memory access time of 6.5 ns? [4]



A multi-tasking system runs ten I/O-bound tasks and one CPU-bound task. Assume that the I/O-bound tasks issue and I/O call once every millisecond of CPU computing and that each I/O operation takes 10 msec to complete. The context switching overhead is 0.1msec and that all processes are long-running tasks. What is the CPU utilization for a round-robin scheduler when the time-slice is: a) 1 msec; b) 10 msec [4]

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What are the various reasons due to which the number of bugs vs. time in a software takes the shape of a bath-tub curve (first decreases, then remains constant for some period and then starts increasing), when plotted with respect to time? [4]



What are the various reasons due to which the failure function of a software takes the shape of a bath-tub curve (first decreases, then remains constant for some period and then starts increasing), when plotted with respect to time? [4]



What are the various reasons due to which the number of bugs in a software first decreases, then remains constant for some period and then starts increasing), when plotted with respect to time? [4]

Q.6 Set (A)

Consider the following three periodic tasks T1, T2, and T3 (having decreasing priority) scheduled under RM. All the critical sections are shown below. Access to semaphores (s1, s2, and s3) is controlled by the Priority Inheritance Protocol. The worst-­‐case execution times of functions g(), h(), and m() are 2, 3, and 4 respectively. The execution times of P() and V() (signal & wait) are assumed to be 0. Please compute the maximum blocking time of each task. [4]

|  |  |  |
| --- | --- | --- |
| *T1:* | *T2:* | *T3:* |
| *…* | *…* | *…* |
| *wait(s1);* | *wait(s1);* | *wait(s2);* |
| *g();* | *h();* | *h();* |
| *signal(s1);* | *signal(s1);* | *signal(s2);* |
| *…* | *…* | *…* |
| *wait(s2);* | *wait(s3);* | *wait(s3);* |
| *g();* | *m();* | *m();* |
| *signal(s2);* | *signal(s3);* | *signal(s3);* |
| *…* |  | *…* |
| *wait(s3);* |  | *wait(s1);* |
| *h();* |  | *m();* |
| *signal(s3);* |  | *signal(s1);* |

Q.6 Set (B)

Consider the following three periodic tasks T1, T2, and T3 (having decreasing priority) scheduled under RM. All the critical sections are shown below. Access to semaphores (s1, s2, and s3) is controlled by the Priority Inheritance Protocol. The worst-­‐case execution times of functions g(), h(), and m() are 2, 3, and 4 respectively. The execution times of P() and V() (signal & wait) are assumed to be 0. Please compute the maximum blocking time of each task. [4]

|  |  |  |
| --- | --- | --- |
| *T1:* | *T2:* | *T3:* |
| *…* | *…* | *…* |
| *wait(s1);* | *wait(s1);* | *wait(s2);* |
| *g();* | *h();* | *h();* |
| *signal(s1);* | *signal(s1);* | *signal(s2);* |
| *…* | *…* | *…* |
| *wait(s2);* | *wait(s3);* | *wait(s3);* |
| *g();* | *m();* | *m();* |
| *signal(s2);* | *signal(s3);* | *signal(s3);* |
| *…* |  | *…* |
| *wait(s3);* |  | *wait(s1);* |
| *h();* |  | *m();* |
| *signal(s3);* |  | *signal(s1);* |

Q.6 Set (C)

Consider the following three periodic tasks T1, T2, and T3 (having decreasing priority) scheduled under RM. All the critical sections are shown below. Access to semaphores (s1, s2, and s3) is controlled by the Priority Inheritance Protocol. The worst-­‐case execution times of functions g(), h(), and m() are 2, 3, and 4 respectively. The execution times of P() and V() (signal & wait) are assumed to be 0. Please compute the maximum blocking time of each task. [4]

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| *T1:* | *T2:* | *T3:* |
| *…* | *…* | *…* |
| *wait(s1);* | *wait(s1);* | *wait(s2);* |
| *g();* | *h();* | *h();* |
| *signal(s1);* | *signal(s1);* | *signal(s2);* |
| *…* | *…* | *…* |
| *wait(s2);* | *wait(s3);* | *wait(s3);* |
| *g();* | *m();* | *m();* |
| *signal(s2);* | *signal(s3);* | *signal(s3);* |
| *…* |  | *…* |
| *wait(s3);* |  | *wait(s1);* |
| *h();* |  | *m();* |
| *signal(s3);* |  | *signal(s1);* |

Q.7 Set (A)  
In an system processing only asynchronous tasks (i.e. there are no periodic tasks running in the system), the mean inter-arrival time of these tasks is 10 ms and average processing time of these tasks is 4 ms. What should be the mean depth of the queue to store these tasks. What is the probability of CPU getting overloaded? [4]

Q.7 Set (B)  
In an system processing only asynchronous tasks (i.e. there are no periodic tasks running in the system), the mean inter-arrival time of these tasks is 10 ms and average processing time of these tasks is 4 ms. What should be the mean depth of the queue to store these tasks. What is the probability of CPU getting overloaded? [4]

Q.7 Set (C)  
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Q.8 Set (A)

Validate the two below statements (True/False) with brief justification:

1. While designing a clock driven schedule for 3 periodic tasks (10,2), (15,4) and (20,5), a designer selected the frame size as ‘4’. Do you agree with the designer’s choice regarding the frame size? Please provide one line justification for your answer.
2. We can use hard-disks in RT systems If we can store files contiguously minimizing R/W Head movements. [4]

Q.8 Set (B)

Validate the two below statements (True/False) with brief justification:

1. While designing a clock driven schedule for 3 periodic tasks (10,2), (15,4) and (20,5), a designer selected the frame size as ‘4’. Do you agree with the designer’s choice regarding the frame size?
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Q.8 Set (C)

1. While designing a clock driven schedule for 3 periodic tasks (10,2), (15,4) and (20,5), a designer selected the frame size as ‘4’. Do you agree with the designer’s choice regarding the frame size?
2. We can use hard-disks in RT systems If we can store files contiguously minimizing R/W Head movements. [4]

Q.9 Set (A)

Identify the following environments as either hard or soft real-time with brief justification for each.

a. Thermostat in a household.

b. Control system for a nuclear power plant.

c. Fuel economy system in an automobile.

d. Landing system in a jet airliner. [4]

Q.9 Set (B)

Identify the following environments as either hard or soft real-time with brief justification for each.

a. Thermostat in a household.

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c. Fuel economy system in an automobile.

d. Landing system in a jet airliner. [4]

Q.9 Set (C)

Identify the following environments as either hard or soft real-time with brief justification for each.

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Q.10 Set (A)  
a) How Fault-Tolerance techniques enhance reliability of Hard RT systems? Give examples of Hardware and Software Fault-tolerance methods.

b) What are the necessary conditions for a deadlock? Can deadlocks occur in non-RT systems? Explain. [4]

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